AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [1067] with the following amended paragraph:

[1067] In the embodiment of the invented memory cell shown in Figure 4(a), there are two explicit local terminals: an input terminal 20 (also called a wordline), and an output terminal 21 (also called a bitline). In addition the cell may also contain "implicit" or "widely shared" terminals which are unavoidable consequences of its construction, and which are common to large groups of cells at once. One example of an implicit terminal is the semiconductor substrate, which forms a parasitic capacitance to each memory cell. To simplify the figures and the discussion, these implicit terminals are omitted, but as will be appreciated these implicit terminals might affect the functionality and performance of the memory cell. Thus the invented memory cell is referred to as a "two terminal structure", meaning there are two explicit, local[[,]] terminals, possibly with additional terminals which are implicit rather than explicit.

Please replace paragraph [1093] with the following amended paragraph:

[1093] In this embodiment, a pillar contains four layers of material in a layer stack, deposited sequentially as shown in Figure 6(a): (1) a layer of P+ doped polysilicon 40; (2) a layer of N- doped polysilicon 41; (3) a layer of silicon dioxide 42; (4) a layer of N+ doped polysilicon 43. Layers (40) and (41) form a PN junction diode (the steering element), and layers (41-43) form a poly-oxide-poly dielectric rupture antifuse. In this embodiment the stack of four materials which together create the memory cells are referred to as the "layer stack" 45. There is ~~are~~ also a conductor layer below and above the layer stack 45 which is patterned as will be described. These are shown as conductors 46 and 48 in Figure 6(a).

Please replace paragraph [1103] with the following amended paragraph:

[1103] Next, the mask which defines the features on the conductors1 layer is applied, and these features are etched into both the pillar layer stack 45 and the conductors1 layer 46 below. An insulator is deposited on the wafer and planarized, using CMP or other planarizing technology. Figure 6(c) shows the wafer at this stage. Note in particular that the pillar layer stack and bottom layer have[[,]] been etched into long continuous strips (46a and 45a) and (46b and 45b), not isolated individual pillars. Also note that the edges of the pillar layer stack 45a and

45b are aligned to the edges of the conductor 46a and 46b layer, since both were etched at the same time with the same mask. Note the conductors generally comprise coplanar conductors, such as aluminum or other metals, silicides, or doped silicon conductors, for each level.

Please replace paragraph [1165] with the following amended paragraph:

[1165] Suppose the first set-select signal is in the select condition (high voltage) and the second set-select signal is in the deselect condition. Then the wordlines on layers conductors1, conductors5, conductors9, ..., etc are driven, while the wordlines on layers conductors3, conductors7, conductors11, ... are not driven. There is only one (unique) path to the bitline on conductors2: ~~conductor2:~~ this is the path from conductors1, through the memory cell between conductors1 and conductors2, ~~conductor2,~~ and onto the bitline on the conductors2 ~~conductor2~~ layer. The other possible path, from conductors3, through the memory cell between conductors3 and conductors2, ~~conductor2,~~ and onto conductors2, ~~conductor2,~~ is disabled because conductors3 is in the second wordline set and is not driven.

Please replace paragraph [1176] with the following amended paragraph:

[1176] In some embodiments, the voltage necessary to program the state change element[[,]] may exceed the voltage capabilities of the peripheral transistors. This is particularly true when the transistors are scaled for small dimensions (for example, channel length below 0.2 microns). In these cases the peripheral circuits may be arranged so that during a write cycle, the row decoders operate from a power supply of +V volts, while the column decoders and column I/O circuits and write data drivers operate from a power supply of –V volts. This arrangement puts a voltage difference of 2xV volts across the memory cell being written ((+V) – (–V) = 2xV), while placing at most V volts across any one transistor.